CLAIMS

1. A driver circuit for controlling upper and lower switching means (T_3, T_4) for converting a direct voltage U_d into a clocked output voltage U_a for a resonant converter with a high-voltage section (HT) for controlling the upper switching means (T_3) and a low-voltage section (NT) for controlling the lower switching means (T_4), which switch the switching means (T_3, T_4) on alternately, the switch-on phases of the switching means (T_3, T_4) being separated from one another by dead-time phases, characterized in that there is provided a first circuit section which controls the duty cycle Δt_{ein3} of the upper switching means (T_3) as a function of the duty cycle Δt_{ein4} of the lower switching means (T_4), and receives control signals from the low-voltage section (NT) exclusively during the duty cycle Δt_{ein4} of the lower switching means (T_4).

2. A driver circuit as claimed in claim 1, characterized in that the first circuit section is equipped with at least one first integrating circuit configuration which is charged during the duty cycle Δt_{ein4} of the lower switching means (T_4), and discharged during the duty cycle Δt_{ein3} of the upper switching means (T_3).

3. A driver circuit as claimed in claim 2, characterized in that the first integrating circuit configuration is equipped with at least one integration capacitor (C_3) and a charging circuit and a discharging circuit.

4. A driver circuit as claimed in claim 3, characterized in that the charging circuit and the discharging circuit are both equipped with a respective constant-current source (I_1, I_2).

5. A driver circuit as claimed in one of claims 2 to 4, characterized by a transistor (T_2) provided in the low-voltage section (NT), which transmits a signal to the high-voltage section (HT) for the duration of the switch-on of the lower switching means (T_4).

6. A driver circuit as claimed in one of claims 1 to 5, characterized by a second circuit section which determines the switch-on instant t_{ein3} of the upper switching means as a function of the voltage characteristic of the output voltage U_a.

7. A driver circuit as claimed in claim 6, characterized in that the second circuit section is equipped with a voltage-increase recognition circuit with at least one capacitor (C_1), one resistor (R_1) and one comparator (G1A), in particular a Schmitt trigger.

8. A driver circuit as claimed in one of claims 1 to 5, characterized by a second circuit section with means which control the duration Δt_{tot1} of the first dead-time phase before the switch-on of the upper switching means (T_3) as a function of the duration Δt_{tot2} of the second dead-time phase before the switch-on of the lower switching means (T_4), or by a timer connected to the low-voltage section (NT).

9. A driver circuit as claimed in claim 8, characterized in that the second circuit section is equipped with at least one second integrating circuit configuration which is charged for the duration Δt_{tot2} of the second dead-time phase, or for the duration of a signal from the external timer, and discharged for the duration Δt_{tot1} of the first dead-time phase.

10. A driver circuit as claimed in claim 9, characterized in that the structure of the second integrating circuit configuration corresponds to the structure of the first integrating circuit configuration.

11. A driver circuit as claimed in one of claims 1 to 10, characterized by a voltage-decrease recognition circuit with at least one capacitor (C_4), one resistor (R_3) and one comparator (G4A), especially a Schmitt trigger, for determining the switch-on instant t_{ein4} for the lower switching means (T_4).

12. A resonant converter with a driver circuit for controlling upper and lower switching means (T_3, T_4) for converting a direct voltage U_d into a clocked output voltage U_a for the resonant converter with a high-voltage section (HT) for controlling the upper switching means (T_3) and a low-voltage section (NT) for controlling the lower switching means (T_4), which switch the switching means (T_3, T_4) on alternately, the switch-on phases of the switching means (T_3, T_4) being separated from one another by dead-time phases,

characterized by a first circuit section, which controls the duty cycle Δt_{ein3} of the upper switching means (T_3) as a function of the duty cycle Δt_{ein4} of the lower switching means (T_4), and receives control signals from the low-voltage section (NT) exclusively during the duty cycle Δt_{ein4} of the lower switching means (T_4).

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